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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,430	10/16/2003	Joseph A. Bennett	P9338C	8033

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EXAMINER	
PHAN, RAYMOND NGAN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 09/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/687,430	BENNETT, JOSEPH A.	
	Examiner	Art Unit	
	Raymond Phan	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5,6,10,11,24,25 and 31-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,10,11,24,25 and 31-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

1. This application has been examined. Claims 1-2, 5-6, 10-11, 24-25, 31-46 are pending.

2. The Group and/or Art Unit location of your application in the PTO has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Group Art Unit 2111.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Suggested title: -- Independent busses coherency maintaining method, involves waiting for tag acknowledge by input/output controller from memory controller before providing notification to processing unit that data writing has completed –

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214

USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 in Patent No. 6,658,520. Although the conflicting claims are not identical, they are not patentably distinct from each other because the omissions of,

> writing the data to the memory from one of at least one DMA controller at the I/O controller;
>
> sending that data from the one of at least one DMA controller to a second memory at the I/O controller and then the writing the data to memory;
>
> sending the data, by the I/O controller, from the second memory via the first bus to a third memory at the memory controller and then the writing the data to the memory; and
>
> sending the tag acknowledgement from the memory controller to the one of at least one DMA controller via the third memory, first bus and the second memory,

in claim 1 are obvious expedients since elements of claim 1 of the present application still perform the same functions,

> writing data from an Input/Output (I/O) controller to a memory, the I/O controller sending the data to the memory via a first bus connected to a first port of a memory controller and the I/O controller;
>
> sending a tag, from the I/O controller, after the data via the first bus through the first port, the tag being received by the memory controller;
>
> requesting completion status of the data write from the I/O controller by a processing unit, the request being sent to the I/O controller via a second bus connected to a second port of the memory controller and the I/O controller; and
>
> waiting for a tag acknowledgment, by the I/O controller, from the memory controller before providing notification to the processing unit that the data write has completed,

as claim 1 of the patent.

6. Claim 10 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 6 in Patent No. 6,658,520. Although the conflicting claims are not identical, they are not patentably distinct from each other because the omissions of,

> a second memory at the memory controller and a third memory at the I/O controller, the data write sent from the I/O controller to the memory via the third memory, first bus, and second memory; and

a fourth memory at the memory controller and a fifth memory at the I/O controller, the processing unitsending a status request to the I/O controller via the fourth memory, second bus, and fifth memory,

in claim 10 are obvious expedients since elements of claim 10 of the present application still performs the same functions,

at least one memory device;

a memory controller operably connected to the at least one memory device;

a processing unit operably connected to the memory controller;

and an Input/Output (I/O) controller operably connected to the memory controller by a first bus and a second bus, the I/O controller writing data to the at least one memory device via the first bus and the memory controller, the I/O controller sending a tag after the memory write to the memory controller via the first bus, the processing unit requesting status from the I/O controller via the memory controller and the second bus,

wherein the I/O controller waits for a tag acknowledgment from the memory controller before providing notification to the processing unit via the second bus that the data write has completed ensuring that the first bus and the second bus are coherent,

as claim 6 of the patent.

7. Claim 24 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 11 in Patent No. 6,658,520. Although the conflicting claims are not identical, they are not patentably distinct from each other because the omissions of,

a second memory at the memory controller and a third memory at the I/O controller, the data write sent from the I/O controller to the memory via the third memory, first bus, and second memory; and

a fourth memory at the memory controller and a fifth memory at the I/O controller, the processing unitsending a status request to the I/O controller via the fourth memory, second bus, and fifth memory,

in claim 24 are obvious expedients since elements of claim 24 of the present application still performs the same functions,

at least one memory device;

a memory controller operably connected to the at least one memory device;

at least one processing unit operably connected to the memory controller;

at least one Input/Output (I/O) controller; at least one first bus, one associated at least one first bus operably connected between one at least one I/O controller and the memory controller;

a second bus operably connected between the memory controller and each at least one I/O controller, each at least one I/O controller writing data to the at least one memory device via the associated at least one first bus and the memory controller, each at least one I/O controller sending a tag after the memory write to the memory controller via the associated first bus, the processing unit requesting status from each at least one I/O controller that initiates the write via the memory controller and the second bus,

wherein each at least one I/O controller waits for a tag acknowledgment from the memory controller before providing notification to the processing unit via the second bus that the data write has completed ensuring that each at least one first bus and the second bus are coherent,

as claim 11 of the patent.

In re Karlson, 136 USPQ 189 (ccPA 1963).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-2, 10, 24-25, 31-46 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kondo et al. (US No 5,671,371) in view of Story et al. (US No. 5,905,912).

In regard to claims 1, 10, 24, Kondo et al. disclose a method for keeping two independent buses coherent comprising writing data from an I/O controller to a memory, the I/O controller sending the data to the memory via a first bus connected to a first port of the memory controller and the I/O controller (see col. 4, liens 18-51); sending a tag, from the I/O controller, after the data via the first bus through the first port, the tag being received by the memory controller (see col. 4, line 56 through col. 5, line 12). But Kondo et al. do not specifically disclose requesting completion status of the data write from the I/O controller by a processing unit, the request being sent to the I/O controller via a second bus connected to a second port of the memory controller and the I/O controller; and waiting for the tag acknowledgement, by the I/O controller, from the memory controller before providing notification to the processing unit that the data write has completed. However Story et al. disclose requesting completion status of the data write from the I/O controller by a processing unit, the request being sent to the

I/O controller via a second bus connected to a second port of the memory controller and the I/O controller (see col. 2, lines 38-62); and waiting for the tag acknowledgement, by the I/O controller, from the memory controller before providing notification to the processing unit that the data write has completed (see col. 2, lines 38-62). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Story et al. within the system of Kondo et al. because it would be able to handle multiple transactions without CPU intervention thereby further enhancing the time savings of the CPU.

In regard to claim 2, Story et al. disclose comprising writing the data to the memory from one of at least one DMA controller at the I/O controller (see col. 4, lines 26-47).

In regard to claims 31, Kondo et al. disclose a method for keeping two independent buses coherent comprising writing data from an I/O controller to a memory, the I/O controller sending the data to the memory via a first bus connected to a first port of the memory controller and the I/O controller (see col. 4, liens 18-51); sending a tag, from the I/O controller, after the data via the first bus through the first port, the tag being received by the memory controller (see col. 4, line 56 through col. 5, line 12). But Kondo et al. do not specifically disclose requesting completion status of the data write from the I/O controller by a processing unit, the request being sent to the I/O controller via a second bus connected to a second port of the memory controller and the I/O controller; and waiting for the tag acknowledgement, by the I/O controller, from the memory controller before providing notification to the processing unit that the data write has completed. However Story et al. disclose requesting completion status of the

data write from the I/O controller by a processing unit, the request being sent to the I/O controller via a second bus connected to a second port of the memory controller and the I/O controller (see col. 2, lines 38-62); and waiting for the tag acknowledgement, by the I/O controller, from the memory controller before providing notification to the processing unit that the data write has completed (see col. 2, lines 38-62). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Story et al. within the system of Kondo et al. because it would be able to handle multiple transactions without CPU intervention thereby further enhancing the time savings of the CPU.

In regard to claims 32, 38, 44, Kondo et al. disclose the step of transferring a fence (i.e. tag) to the memory controller via the first bus that request the memory controller to send the notification (see col. 4, line 56 through col. 5, line 12).

In regard to claims 33, 36, 39, 42, 45, Story et al. disclose the step of receiving from the processor via the second bus the status request for the data before providing the processor with the completion status completed (see col. 2, lines 38-62). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Story et al. within the system of Kondo et al. because it would be able to handle multiple transactions without CPU intervention thereby further enhancing the time savings of the CPU.

In regard to claims 34, 41, 46, Story et al. disclose the step of receiving configuration information from the processor via the second bus that configures the I/O controller to write the data to the memory via the first bus and the memory controller (see col. 2, line 63 through col. 3, line 13). Therefore, it would have been

obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Story et al. within the system of Kondo et al. because it would be able to handle multiple transactions without CPU intervention thereby further enhancing the time savings of the CPU.

In regard to claim 35, Kondo et al. disclose the step of transferring a fence (i.e. tag) to the memory controller via the first bus that request the memory controller to send the notification (see col. 4, line 56 through col. 5, line 12). But Kondo et al. do not disclose step of receiving from the processor via the second bus the status request for the data before providing the processor with the completion status completed; step of receiving configuration information from the processor via the second bus that configures the I/O controller to write the data to the memory via the first bus and the memory controller. However Story et al. disclose step of receiving from the processor via the second bus the status request for the data before providing the processor with the completion status completed (see col. 2, lines 38-62); step of receiving configuration information from the processor via the second bus that configures the I/O controller to write the data to the memory via the first bus and the memory controller (see col. 2, line 63 through col. 3, line 13). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Story et al. within the system of Kondo et al. because it would be able to handle multiple transactions without CPU intervention thereby further enhancing the time savings of the CPU.

In regard to claim 37, 40, 43, Kondo et al. disclose a method for keeping two independent buses coherent comprising writing data from an I/O controller to a memory, the I/O controller sending the data to the memory via a first bus

connected to a first port of the memory controller and the I/O controller (see col. 4, liens 18-51); sending a tag, from the I/O controller, after the data via the first bus through the first port, the tag being received by the memory controller (see col. 4, line 56 through col. 5, line 12). But Kondo et al. do not specifically disclose requesting completion status of the data write from the I/O controller by a processing unit, the request being sent to the I/O controller via a second bus connected to a second port of the memory controller and the I/O controller; and waiting for the tag acknowledgement, by the I/O controller, from the memory controller before providing notification to the processing unit that the data write has completed; step of receiving configuration information from the processor via the second bus that configures the I/O controller to write the data to the memory via the first bus and the memory controller. However Story et al. disclose requesting completion status of the data write from the I/O controller by a processing unit, the request being sent to the I/O controller via a second bus connected to a second port of the memory controller and the I/O controller (see col. 2, lines 38-62); and waiting for the tag acknowledgement, by the I/O controller, from the memory controller before providing notification to the processing unit that the data write has completed (see col. 2, lines 38-62); step of receiving configuration information from the processor via the second bus that configures the I/O controller to write the data to the memory via the first bus and the memory controller (see col. 2, line 63 through col. 3, line 13). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Story et al. within the system of Kondo et al. because it would be able to handle multiple transactions without CPU intervention thereby further enhancing the time savings of the CPU.

10. Claims 5-6, 11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kondo et al. in view of Story et al. and further in view of Suzuki (US No. 6,240,481).

In regard to claim 5, Kondo et al. and Story et al. teach the claimed subject matter as discussed above except the teaching of sending the data from the one of at least one DMA controller to the second memory at the I/O controller and then the writing the data to memory. However Suzuki disclose sending the data from the one of at least one DMA controller to the second memory at the I/O controller and then the writing the data to memory (see col. 9, line 45 through col. 10, line 9). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Suzuki within the system of Kondo et al. and Story et al. because it would provide an interface apparatus and a data processing system wherein load of data processing for control apparatus in system superiority can be reduced in term of data transmission.

In regard to claims 6, 11,Suzuki discloses further comprising sending the data by the I/O controller, from the second memory via the first bus to the third memory at the memory controller and then the writing the data to memory (see col. 10, lines 9-32). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Suzuki within the system of Kondo et al. and Story et al. because it would provide an interface apparatus and a data processing system wherein load of data processing for control apparatus in system superiority can be reduced in term of data transmission.

Conclusion

11. Claims 1-2, 5-6, 10-11, 24-25, 31-46 are rejected.

12. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.

Bridges et al. (US No. 6,055,584) disclose a processor local bus posted DMA flyby burst transfers.

Taglione et al. (US No. 6,061,748) disclose a method and apparatus for moving data packets between networks while minimizing CPU intervention using a multi-bus architecture having DMA bus.

Yamamoto (US No. 6,453,368) discloses an adding a dummy data or discarding a portion of data in a bus repeater buffer memory for a second data transfer to a second bus.

Green, III et al. (US No. 6,047,336) disclose a speculative DMA transfer between slave devices and memory.

Takahashi (US No. 6,249,833) discloses a dual bus processing apparatus wherein second control means request access of first data bus from first control means while occupying second data bus.

Hayashi (US No. 6,269,102) discloses a bus control device.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (703) 306-2756. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Primary, Paul Myers can be reached on (703) 305-9656 or via e-mail addressed to paul.myers@uspto.gov. The fax phone number for this Group is (703) 746-7239.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**raymond.phan@uspto.gov**].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35

U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Paul R. Myers

PAUL R. MYERS
PRIMARY EXAMINER

Raymond Phan
9/21/04